IN THE SPECIFICATION

Replace the first two paragraphs on page 1 with the following amended two paragraphs:

This application claims priority to European Application Serial No. 00402331.3, filed August 21, 2000 (TI-31366EU) and to European Application Serial No. 01401218.1, filed May 11, 2001 (TI-31357EU). US Patent Application Serial No. [_____] 09/932,651 (TI-31366US) is incorporated herein by reference.

Co-Related Applications

This application is related to patent application Serial No. [_____] 09/932,397 (TI-31355), entitled *TLB Operation Based on Task-ID*; patent application Serial No. [_____] 09/932,382 (TI-31356), entitled *TLB Lock and Unlock Operation*; and patent application Serial No. [_____] 09/932,611 (TI-31358), entitled *TLB with Resource ID Field.*

Replace paragraph 52 with the following amended paragraph:

[52] A processor can initiate various control operations on a TLB by writing a control word conforming to appropriate format to a specific memory mapped address associated with TLB controller 320. This control word can specify a target virtual address entry and an associated task ID or an associated resource ID. Depending on the operation, unneeded fields are ignored. For example, the operation "invalidate all entries related to an R-ID" will only use the R-ID field 404. The format and type of operation can be distinguished by using different memory mapped addresses, for example. Each address corresponds to a different TLB operation. Another embodiment would be to use a different processor instruction opcode for each of the TLB operation that would drive the appropriate control signal connected to TLB controller 2232 which will be described in more detail with respect to Figure 7. A state machine in TLB controller 320 then executes the requested control operation. These TLB control operations are listed in Table 5. These operations are described in more detail below. For many of the operations, certain processors in an embodiment will be restricted to only affecting their own entries. This restriction is enforced by using the resource-ID signals 2106 (illustrated in Figure 6) provided with each write to TLB controller 320 as part of each memory access request.

Replace paragraph 73 with the following amended paragraph:

[73] Figure 6 is a simplified block diagram of the TLB of Figure 3A and will now be referred to explain selective invalidation of an entry for a given task or resource, as listed in Table 5. Processor 2100(m) is representative of one or more requestors that access TLB 2130. A physical address bus 2104(m), resource ID signals 2106(m), and task ID signals 2108(m[[n]]) are provided by each processor 2100(m[[n)]]) for each TLB request. Traffic controller 2110 provides request priority selection and sends the highest priority request to TLB 2130 using physical address bus 2104, resource ID signals 2106, and task ID signals 2108 to completely identify each request.